Claims

1. A system (1) comprising
- a first semiconductor device (2a), and
- a second semiconductor device (2b),
wherein the first semiconductor device (2a) comprises a voltage supply means (3a),
characterized in that said voltage supply means (3a) of said first semiconductor device (2a) is connected to said second semiconductor device (2b), so that said voltage supply means (3a) of said first semiconductor device (2a) can provide a supply voltage for said second semiconductor device (2b).

2. The system (1) according to claim 1, wherein said first semiconductor device (2a) and said second semiconductor device (2b) are arranged in the same housing (4).

3. The system (1) according to claim 2, wherein said first and second semiconductor devices (2a, 2b) are arranged in said housing (4) in a stacked manner.

4. The system (1) according to claims 2 or 3, wherein said housing (4) is a plug mountable semiconductor device housing.

5. The system (1) according to claim 4, wherein said plug mountable semiconductor device housing is a Dual-In-Line (DIL) housing.

6. The system (1) according to claim 4, wherein said plug mountable semiconductor device housing is a Pin-Grid-Array (PGA) housing.

7. The system (1) according to claims 2 or 3, wherein said housing (4) is a surface mountable semiconductor device housing.

8. The system (1) according to any of the preceding claims, said system comprising one or several further semiconductor devices.

9. The system (1) according to claim 8, wherein said one or said several further semiconductor device(s) is/are arranged in the same housing (4), in particular in the same semiconductor device housing, as are said first and said second semiconductor devices (2a, 2b).

10. The system according to claims 8 or 9, wherein said voltage supply means (3a) of said first semiconductor device (2a) is additionally also connected to said one or to said several further semiconductor device(s), so that said voltage supply means (3a) of said first semiconductor device (2a) can additionally provide a supply voltage for said one or said several further semiconductor device(s).

11. The system (1) according to any of claims 8 or 9, wherein said first semiconductor device (2a) comprises a further voltage supply means that is connected to said one or said several further semiconductor device(s), so that said further voltage supply means of said first semiconductor device (2a) can provide a supply voltage for said one or said several further semiconductor device(s).

12. The system (1) according to any of the preceding claims, wherein said first and/or said second semiconductor devices (2a, 2b), and/or said one and/or said several further semiconductor devices are memory devices.

13. The system (1) according to claim 12, wherein said memory device is a table memory device or said memory devices (2a, 2b) are table memory devices, respectively.

14. The system (1) according to claim 13, wherein said table memory device is a RAM table memory device or said table memory devices are RAM table memory devices, respectively.

15. The system (1) according to claim 14, wherein said RAM table memory device is a DRAM table memory device or said RAM table memory devices are DRAM table memory devices, respectively.

16. The system (1) according to claim 13, wherein said table memory device is a ROM table memory device or said table memory devices are ROM table memory devices, respectively.

17. The system (1) according to claim 12, wherein said memory device is a functional memory device or said memory devices are functional memory devices, respectively, in particular PLDs and/or PLAs.

18. The system (1) according to any of the preceding claims, wherein said voltage supply means (3a) and/or said further voltage supply means provide a voltage supply for said first semiconductor device (2a).

19. The system (1) according to any of the preceding claims, wherein said voltage supply means (3a) and/or said further voltage supply means generate(s) the respective supply voltage from an external voltage.

20. The system (1) according to any of the preceding claims, wherein said voltage supply means (3a) and/or said further voltage supply means are or comprise a voltage regulating means.

21. The system (1) according to any of the preceding claims, wherein said voltage supply means (3a) and/or said further voltage supply means are or comprise a charge pump.

22. The system (1) according to any of the preceding claims, wherein said second semiconductor device (2b) comprises a voltage supply means (3b), and wherein, in a first operating mode of said second semiconductor device (2b), said voltage supply means (3b) of said second semiconductor device (2b) provides the supply voltage for said second semiconductor device (2b), and wherein, in a second operating mode of said second semiconductor device (2b), said voltage supply means (3a) of said first semiconductor device (2a) provides the supply voltage for said second semiconductor device (2b).

23. The system (1) according to claim 22, wherein said voltage supply means (3b) of said second semiconductor device (2b) is activated in the first operating mode, and wherein said supply voltage means (3b) of said second semiconductor device (2b) is deactivated in the second operating mode.

24. The system (1) according to claims 22 or 23, wherein the second operating mode is a standby mode.

25. The system (1) according to claims 22, 23, or 24, wherein the second operating mode is a refresh mode.

26. The system (1) according to any of claims 22 to 25, wherein the first operating mode is a working mode, in particular a mode in which external access to the second semiconductor device (2b) is performed.

27. The system (1) according to any of the preceding claims, wherein a device function adjusting means, in particular an appropriate fuse, is provided on said first and/or second semiconductor device(s) (2a, 2b), by means of which it is determined whether the corresponding semiconductor device (2a,

2b) is to assume the function of said first semiconductor device (2a) or the function of said second semiconductor device (2b).

28. The system (1) according to any of the preceding claims, wherein said voltage supply means (3a) of said first semiconductor device (2a) is connected to a corresponding pad (5a) of said first semiconductor device (2a).

29. The system (1) according to claim 28, wherein said pad (5a) of said first semiconductor device (2a) is connected to a corresponding pad (5b) of said second semiconductor device (2b), in particular to a pad (5b) which said voltage supply means (3b) of said second semiconductor device (2b) can be connected to.

30. The system (1) according to claim 29, wherein said pad (5a) of said first semiconductor device (2a) is connected directly to the corresponding pad (5b) of said second semiconductor device (2b), in particular by means of an appropriate bonding wire (6).

31. The system (1) according to claim 29, wherein said pad (5a) of said first semiconductor device (2a) is connected indirectly to the corresponding pad (5b) of said second semiconductor device (2b), in particular via an interposer (9).